

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	((("6319784") or ("6506647"))).PN	US-PGPUB; USPAT	OR	OFF	2004/12/14 13:43
L2	2858	(MISFET or MOSFET) and (trench near3 isolation) and (clean or remove or cleaning or removing)	US-PGPUB; USPAT	OR	ON	2004/12/14 16:29
L3	2175	2 and @ad<"20020719"	US-PGPUB; USPAT	OR	ON	2004/12/14 16:29
L4	567	3 and (HF or "NH.sub.4F")	US-PGPUB; USPAT	OR	ON	2004/12/14 16:30
L5	50	(MISFET or MOSFET) and (trench near3 isolation) and (clean or remove or cleaning or removing)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/14 16:33
L7	612	(protected or protecting or protect or protection or protective) with (isolation near3 trench)	US-PGPUB; USPAT	OR	ON	2004/12/14 16:33
L8	106	7 and (MISFET or MOSFET)and (clean or remove or cleaning or removing)	US-PGPUB; USPAT	OR	ON	2004/12/14 16:33
L9	85	8 and @ad<"20020719"	US-PGPUB; USPAT	OR	ON	2004/12/14 16:29
L10	68	9 not 4	US-PGPUB; USPAT	OR	ON	2004/12/14 16:30
L11	169	(protected or protecting or protect or protection or protective) with (isolation near3 trench)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/14 16:33
L12	50	5 and (MISFET or MOSFET)and (clean or remove or cleaning or removing)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/14 16:33
L14	0	12 not 5	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/14 16:34

US-PAT-NO: 6613636

DOCUMENT-IDENTIFIER: US 6613636 B2

TITLE: Method for fabricating semiconductor device

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Abstract Text - ABTX (1):

On the sides of a gate electrode, layered-film sidewalls are formed which includes a first oxide film such as an NSG film or a TEOS film and a second oxide film such as a BPSG film or a PSG film. After the layered-film sidewalls are used as a mask for forming source and drain regions of a MIS transistor, the second oxide film of the sidewalls is selectively removed. At the removal, wet etching is performed with an aqueous solution containing hydrofluoric acid, and acetic acid or isopropyl alcohol. This makes etching selectivity between oxide films higher and removes only the upper second oxide film. As a result, in the formation of two types of oxide films which differ in their etching properties, the etching selectivity can be prevented from deteriorating.

Application Filing Date - AD (1):

20020522

Brief Summary Text - BSTX (5):

To cope with the above problem, the process described below has been adopted. First, a silicon dioxide (SiO_2 , referred hereinafter to as NSG) film is deposited on the top and sides of a gate electrode by an atmospheric pressure CVD (referred hereinafter to as APCVD) method. Next, a silicon nitride (Si_3N_4 , referred hereinafter to as SiN) film is deposited on the NSG film by a low pressure CVD (referred hereinafter to as LPCVD) method, and a boro-phospho-silicate glass (referred hereinafter to as BPSG)

film or a phospho-silicate glass (referred hereinafter to as PSG) film is then deposited on the SiN film by the APCVD method. The deposited films are etched back, thereby forming sidewalls made of a multi-layered film with a BPSG or PSG/SiN/NSG film structure on the sides of the gate electrode. Accordingly, multi-layered-film sidewalls are obtained which have a structure in which a BPSG (or PSG) film with sectoral cross section is layered on a double-layered film made of NSG and SiN films with substantially L-shaped cross section. Thereafter, the multi-layered-film sidewalls are used as a mask for ion implanting to carry out an ion implantation step for the formation of source and drain regions. Then, in order to widen the space between gate electrodes, the BPSG or PSG films of the multi-layered-film sidewalls are removed selectively by vapor hydrogen fluoride (HF) etching. As a result, only the double-layered film made of NSG and SiN films with substantially L-shaped cross section remains on the sides of the gate electrode, and hence, a wide space is left between the gate electrodes. Accordingly, this process can ensure gap-fill capability of an interlayer dielectric film which will be buried between the gate electrodes.

Brief Summary Text - BSTX (6):

The above-mentioned selective etching of the BPSG (PSG) film by vapor HF etching makes use of the critical concentration of HF for reaction (critical HF concentration for reaction) which varies with the moisture content in an oxide film as a parameter. That is, an oxide film is etched with HF of higher concentration than its critical HF concentration for reaction generally but not etched with HF of lower concentration than its critical HF concentration for reaction. Furthermore, the critical HF concentration for reaction differs depending upon the type of oxide film. Therefore, by vapor-etching the

multi-layered film with HF having a concentration higher than the critical HF concentration for reaction with respect to the BPSG (or PSG) film and lower than the critical HF concentration for reaction with respect to the NSG film, only the BPSG (or PSG) film with sectoral cross section can be removed selectively without etching the almost entire NSG film of substantially L-shape. In addition, the etching selectivity of an oxide film with respect to a SiN film is high, and hence the substantially L-shaped SiN film is hardly etched.

Brief Summary Text - BSTX (7):

For an oxide film exposed to an atmosphere of the dry-etching process or the ion implantation process, however, so-called process damage to its surface layer is caused. The oxide film having such process damage may be etched with HF having a concentration which is lower than its critical HF concentration for reaction and at which a normal oxide film would not be etched.

Brief Summary Text - BSTX (8):

Accordingly, even if only a BPSG (or PSG) film of multi-layered-film sidewalls is intended to be selectively removed by vapor HF etching, the surface of a substantially L-shaped NSG film might be removed at the same time.

Brief Summary Text - BSTX (9):

FIG. 3(a) is a cross sectional view illustrating the shapes of double-layered-film sidewalls after vapor HF etching is carried out according to the conventional process. As shown in FIG. 3(a), due to HF with a lower concentration than the proper critical HF concentration for reaction with respect to an NSG film, the side etching of the NSG film occurs at its damaged portion. This involves the inconvenience that a sufficient etching selectivity of a BPSG (or PSG) film cannot be obtained with respect to an NSG film, and therefore it is difficult to obtain sidewalls of desired shape.

Brief Summary Text - BSTX (11):

Further, when the removal of the BPSG (or PSG) film is made by wet etching with commonly used hydrofluoric acid or buffered hydrogen fluoride, change in etching rate of an oxide film depending upon the existence of process damage is smaller as compared with the vapor HF etching mentioned above. However, hydrofluoric acid and buffered hydrogen fluoride originally have small etching selectivity with respect to different types of oxide film, and then the removal of the entire BPSG (or PSG) film causes an increased amount of side etch of the NSG film.

Brief Summary Text - BSTX (15):

Specifically, a first method for fabricating a semiconductor device of the present invention is directed to a fabrication process of a semiconductor device having a MIS transistor provided with a gate insulating film on a semiconductor substrate and a gate electrode on the film, and includes the steps of: (a) forming, on the sides of the gate electrode, sidewalls including a first oxide film and a second oxide film which have different etching properties; (b) implanting ions for forming source and drain regions using the sidewalls as a mask; and (c) selectively removing the second oxide film by etching the sidewalls with a mixed solution containing hydrofluoric acid and an organic solution.

Brief Summary Text - BSTX (20):

The method further includes the step of cleaning the substrate with a hydrogen peroxide solution or an ozone solution after the step (c) and before a drying step. As a result, a stable chemical oxide film is formed on the surface of the substrate, and the occurrence of stains is suppressed.

Brief Summary Text - BSTX (23):

A second method for fabricating a semiconductor device of the

present

invention includes the steps of: (a) forming, on a substrate, a layered film

including two types of oxide films which differ in their etching properties;

and (b) selectively removing the layered film by selective etching with a mixed

solution containing hydrofluoric acid and an organic solution.

Further in the

step (b), the etching selectivity of one of the two oxide films with respect to

the other is increased using the mixed solution.

Brief Summary Text - BSTX (26):

A third method for fabricating a semiconductor device of the present

invention is directed to a fabrication process of fabricating a semiconductor

device having a MIS transistor, and includes the steps of: (a) forming a gate

oxide film on a surface of a semiconductor substrate; (b) forming a gate

electrode on the gate oxide film with almost all the gate oxide film left; (c)

forming, on the sides of the gate electrode, sidewalls including an oxide film

with different etching properties from the gate oxide film and removing exposed

portion of the gate oxide film; (d) implanting ions for forming source and

drain regions using the sidewalls as a mask; (e) etching the sidewalls with a

mixed solution containing hydrofluoric acid and an organic solution; and (f)

cleaning the semiconductor substrate with a hydrogen peroxide solution or an

ozone solution after the step (e).

Drawing Description Text - DRTX (4):

FIGS. 3(a) and 3(b) are cross sectional views of MISFETs in which how SiN

and NSG films remain after the step shown in FIG. 2(d) is shown by comparing a

conventional example with the above embodiment of the invention.

Detailed Description Text - DETX (12):

FIGS. 2(a) through 2(d) are cross sectional views illustrating process steps

according to an embodiment of the invention. Further, FIGS. 3(a) and 3(b) are

cross sectional views of MISFETs in which how the SiN and NSG films remain after the step shown in FIG. 2(d) is shown by comparing a conventional example with the present embodiment.

Detailed Description Text - DETX (13):

First, in the step shown in FIG. 2(a), th--SiO.sub.2 films 2 (referred hereinafter to as isolation oxide films) are formed on a silicon substrate 1 in isolation regions formed by shallow trench isolation (referred hereinafter to as STI), which defines an n-type MISFET forming region R.sub.nmis at an n-well 3 and a p-type MISFET forming region R.sub.pmis at a p-well 4. Subsequently, a gate insulating film 5 made of a th--SiO.sub.2 film, a polysilicon film 6, a barrier metal film 7 made of titanium nitride (TiN), tungsten nitride (WN) or the like, a high-melting-point metal film 8 made of a tungsten (W) film or the like and a SiN film 9 are deposited in this order on the silicon substrate 1.

Detailed Description Text - DETX (14):

Next, in the step shown in FIG. 2(b), the SiN film 9 is etched by using a photoresist pattern (not shown) for covering a gate electrode forming region, and then the photoresist pattern is removed by ashing. Thereafter, by using the patterned SiN film 9 as a hard mask, the high-melting-point metal film 8, the barrier metal film 7, the polysilicon film 6 and the gate insulating film 5 are patterned. This forms a polymetal gate electrode made of the polysilicon film 6, the barrier metal film 7 and the high-melting-point metal film 8 on each of the n-type MISFET forming region R.sub.nmis and the p-type MISFET forming region R.sub.pmis, through the gate insulating film 5.

Detailed Description Text - DETX (19):

Next, in the step shown in FIG. 2(d), after a photo lithography step and an ion implantation step are completed, a p-type doped layer 13 and an n-type

doped layer 14 are formed as doped surface layers serving as source and drain regions. Further, the BPSG film 12 is selectively removed by wet etching, so that an n-type MISFET and a p-type MISFET are formed which have the SiN film 11 and the NSG film 10 on the sides of the polycrystalline gate electrode.

Detailed Description Text - DETX (20):

In this case, if the oxide films are etched by the conventional vapor ~~xxx~~ etching, the NSG film is partially etched at the removal of the BPSG film to cause a side-etched portion as shown in FIG. 3(a) because the etching selectivity of the BPSG film with respect to the NSG film becomes small due to process damage to the oxide films. Moreover, though not shown in FIG. 3(a), if silicide is formed at the side-etched portion of the NSG film in a later silicide forming step, electric failure such as contact of the silicide layer with a channel region might be caused.

Claims Text - CLTX (1):

1. A method for fabricating a semiconductor device having a MIS transistor provided with a gate insulating film on a semiconductor substrate and a gate electrode on the gate insulating film, the method including the steps of: (a) forming, on the sides of the gate electrode, sidewalls including a first oxide film and a second oxide film which have different etching properties; (b) implanting ions for forming source and drain regions using the sidewalls as a mask; and (c) selectively removing the second oxide film by etching the sidewalls with a mixed solution containing hydrofluoric acid and an organic solution.

Claims Text - CLTX (6):

6. The method of claim 1, wherein the method further includes the step of cleaning the substrate with a hydrogen peroxide solution or an ozone solution after the step (c) and before a drying step.

Claims Text - CLTX (10):

10. A method for fabricating a semiconductor device, including the steps of: (a) forming, on a substrate, a layered film including two types of oxide films which differ in their etching properties; and (b) selectively removing the layered film by selective etching with a mixed solution containing hydrofluoric acid and an organic solution, wherein in the step (b), the etching selectivity of one of the two oxide films with respect to the other is increased using the mixed solution.

Claims Text - CLTX (13):

13. A method for fabricating a semiconductor device having a MIS transistor, the method including the steps of: (a) forming a gate oxide film on a surface of a semiconductor substrate; (b) forming a gate electrode on the gate oxide film with the almost all the gate oxide film left; (c) forming, on the sides of the gate electrode, sidewalls including an oxide film with different etching properties from the gate oxide film and removing exposed portion of the gate oxide film; (d) implanting ions for forming source and drain regions using the sidewalls as a mask; (e) etching the sidewalls with a mixed solution containing hydrofluoric acid and an organic solution; and (f) cleaning the semiconductor substrate with a hydrogen peroxide solution or an ozone solution after the step (e).